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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/702,042	11/06/2003	Jean-Paul Clavequin	003921.00149	7422

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EXAMINER	
STOYNOV, STEFAN	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 11/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/702,042	CLAVEQUIN ET AL.	
	Examiner	Art Unit	
	Stefan Stoynov	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *11* is/are withdrawn from consideration.

5)☒ Claim(s) *1-10 and 12-14* is/are allowed.

6)☒ Claim(s) *15-20 and 22-24* is/are rejected.

7)☒ Claim(s) *21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/06/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Election/Restrictions

Claim 11 is withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 09/05/2006.

Drawings

The drawings are objected to because the contents of Figures 23-45 does not match the description in the specification, starting with paragraph 73, page 22. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 15 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Kent, US Patent No. 5,532,632. Kent discloses all claim elements in Figures 1-4.

Regarding claim 15, Kent discloses a system on a chip synchronizing incoming data with clock, comprising:

a sampling portion (FIG. 1, 42 and 44) configured to sample the incoming data at transition edges of the clock (paragraph 4, lines 32-34);

a decision portion (FIG. 1, 46 and 48) coupled to the sampling portion (FIG. 1, 42 and 44) and configured to decide whether to increase, decrease or maintain the delay amount based on an output of the sampling portion (column 4, lines 43-56); and

a programmable delay (FIG. 1, 18) coupled to the decision portion (via delay counter 20, FIG. 1) and configured to delay the incoming data by the delay amount (column 2, lines 25-35).

Regarding claim 16, Kent further discloses the system, further including a smoothing portion (FIG. 1, 20) coupled to the decision portion and the programmable delay portion (FIG. 1) and configured to increase, decrease, or

maintain the delay amount (column 2, lines 31-47, column 4, lines 43-56) based on at least two sequential decisions by the decisions by the decision portion (sampling the data during two predetermined time intervals on either side of the active edge of the sampling clock – i.e. during NEAR-EARLY and NAER-LATE intervals in sequence, column 2, lines 41-47, column 4, lines 26-30, lines 43-56, FIG(s) 1 and 4).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 17-20 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meier et al., US Patent No. 6,665,218 in view of Kirihata et al, US patent No. 6,636,978. Meier and Kirihata disclose all claim limitations in Figures 1-6 and Figures 1-22, respectively.

Regarding claim 17, Meier discloses a receiver on a chip, comprising:

a digital phase adjustment unit (Phase Detector 135, FIG. 3) configured to adjust a delay of incoming data to the chip, the digital phase adjustment unit periodically increasing and decreasing the delay depending upon values of the incoming data at transition edges of a clock (column 3, lines 12-17, column 4, lines 16-27, lines 45-57).

a controller (Controller 140, FIG. 3) configured to control operations of the digital phase adjustment unit clock (column 4, lines 16-27, lines 45-49)

Meier fails to disclose a latency adjustment unit coupled to the digital phase adjustment unit, configured to adjust for a difference between an expected latency of the incoming data and an actual latency of the incoming data. Meier also fails to disclose the controller configured to control operations of the latency adjustment unit.

Kirihata teaches a digital latency detection circuit (FIG. 8, 840) detecting the digital shift, in particular whether the actual latency coincide with the predetermined latency and generates the corresponding offset signal to be used a command /latency rescheduling circuit (i.e. a controller) (FIG. 8, 850) to adjust the latency shift difference in the data between the drives and the receiver (column 6, lines 10-13, lines 22-41). In Kirihata, the rescheduling scheme implemented with the latency detection circuit and the command/latency rescheduling overcomes a digital latency shift problem in a chip-to-chip communication similar to applicant's invention (column 4, lines 22-31). Thus, any digital latency shifts at any frequency are detected and compensated for (column 4, lines 32-34).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the above described circuit and method, as suggested by Kirihata with the circuit disclosed by Meier in order to implement latency adjustment unit coupled to the digital phase adjustment unit, configured to adjust for a difference between an expected latency of the incoming data and an actual latency of the incoming data, and the controller configured to control operations of the latency adjustment unit. One of ordinary skill in the art would be motivated to do so in order to adjust for the digital latency shifts at any inter-chip frequency.

Regarding claim 18, Meier further discloses the circuit, further including a feedback loop between an output and an input of the digital phase adjustment unit (FIG. 3, feedback loop from the output of Delay Circuit 125 to the Phase Detector 135), the digital phase adjustment unit using a feedback loop to determine an initial amount of delay (column 4, lines 43-49, FIG. 4).

Regarding claim 19, Meier further discloses the circuit as per claim 18, wherein the initial amount of delay depends upon a period of the clock (column 4, lines 33-49).

Regarding claim 20, Meier further discloses the circuit as per claim 18, wherein the initial amount of delay is approximately 0.75 of a period of the clock (FIG. 4).

Regarding claim 22, Kirihata further teaches the controller configured to send a message (SFT_{IN}, SFT_{OUT}, FIG. 8) to the latency adjustment unit, the message including a value of the expected latency (column 6, lines 22-41).

Regarding claim 23, Meier further discloses the circuit, wherein the digital phase adjustment unit includes a pointer that points to an amount of delay (phase shift signal 155, FIG. 3), the pointer moving as the delay is increased and decreased (column 4, lines 16-27).

Regarding claim 24, Meier and Kirihata further teach the circuit, wherein the controller is configured to control the digital phase adjustment unit to generate an initial amount of the delay (Controller 140 controls the delay based on the Phase Detector 135 receiving a feedback signal indicative of the initial delay produced by the Delay Circuit 125, FIG. 3 – column 4, lines 16-27, lines 43-49).

Allowable Subject Matter

Claims 1-14 are allowed.

Claim 21 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim claims 1 and 12, Baba, US Patent Appl. Pub. No. 2003/0219090 teaches comparing an input clock signal with the leading and the trailing edge of an input data signal by data sampling at both clock edges (paragraph 0012, lines 1-17, FIG(s) 7A-9D). Further, Baba teaches the comparator including a plurality of flip-flops to achieve the above-described functionality (paragraph 0045, line 1 – paragraph 0053, line 9, FIG. 6). However,

Baba does not teach the sampling steps, nor does Baba teach the order for executing these steps as required by claim 1. In addition, Baba does not teach or suggest the required interconnections between the different registers and their functionality, as claimed in claim 12.

Simkins et al., US Patent No. 6,690,210 teaches a method and apparatus for data sampling having a delay line and a plurality of tap circuits used for sampling the input data (Abstract, lines 1-8, FIG. 1). However, Simkins does not teach or suggest neither the method steps, nor the element interconnections and their functionality, as indicated in claims 1 and 12.

The Applicant's Admitted Prior art teaches oversampling the incoming data with four different clocks and choosing the most appropriate clock for synchronization. There is no mention of delaying the incoming data as a result of the oversampling.

Claim 21 recites the same method steps, as in claim 1.

Thus, the prior art of record fails to disclose or suggest all the subject matter of claims 1, 12, and 21, including the method steps and the order of execution of these method steps (with regards to claims 1 and 21) and the claimed interconnection of registers and their functionality (required by claim 12).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoynov whose telephone number is (571) 272-4236. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
11/20/06